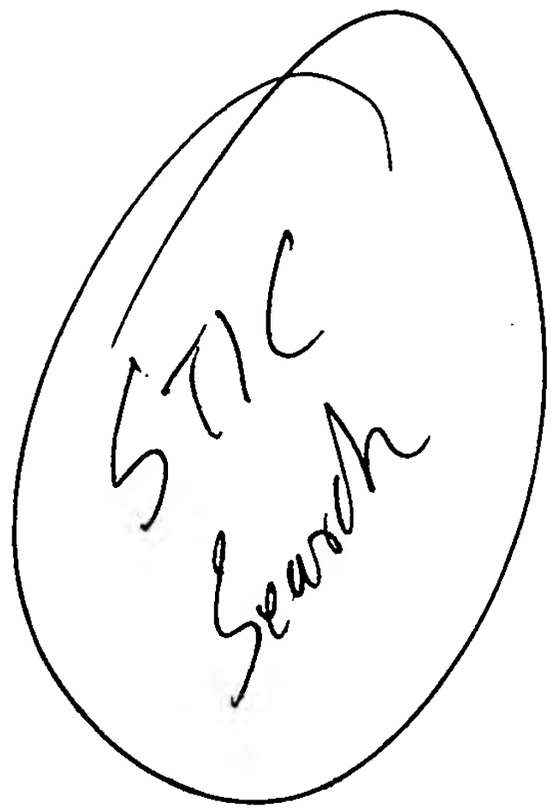
6/15/2006 1:14:18 PM
6/15/2006 1:53:18 PM

[File 2] INSPEC 1898-2006/Jan W2
[File 6] NTIS 1964-2006/Jan W4
[File 8] Ei Compendex(R) 1970-2006/Jan W4
[File 34] SciSearch(R) Cited Ref Sci 1990-2006/Jan W4
[File 434] SciSearch(R) Cited Ref Sci 1974-1989/Dec
[File 35] Dissertation Abs Online 1861-2006/Jan
[File 65] Inside Conferences 1993-2006/Jan W5
[File 94] JICST-EPlus 1985-2006/Nov W3
[File 99] Wilson Appl. Sci & Tech Abs 1983-2006/Apr
[File 144] Pascal 1973-2006/Jan W2
[File 23] CSA Technology Research Database 1963-2006/Jan
[File 103] Energy SciTec 1974-2006/Jan B1
[File 31] World Surface Coatings Abs 1976-2006/Jan
[File 95] TEME-Technology & Management 1989-2006/Jan W5
[File 56] Computer and Information Systems Abstracts 1966-2006/Jun
[File 57] Electronics & Communications Abstracts 1966-2006/Jun
[File 68] Solid State & Superconductivity Abstracts 1966-2006/Jan
[File 60] ANTE: Abstracts in New Tech & Engineer 1966-2006/Jan
[File 293] Engineered Materials Abstracts 1966-2006/Jan
[File 239] Mathsci 1940-2005/Feb
[File 256] TECINFOSOURCE 82-2005/DEC



Set	Items	Description
S1	942858	S LCD? ? OR LIQUID()CRYSTAL()(DISPLAY????? OR PANEL????? OR MATRI????? OR SCREEN? ?) OR (FLAT OR PASSIVE OR ACTIVE)(2N)(DISPLAY???? OR PANEL???? OR MATRI???? OR SCREEN? ?) OR LIQUID(2N)CRYSTAL OR LCM OR DISPLAY(2N)(MEANS OR DEVICE? ? OR APPARATUS OR APPT? ?) OR FED? ? OR FIELD()(EMIS????? OR EMIT?????)()(DISPLAY????? OR PANEL????? OR MATRI??????? OR SCREEN? ?) OR PDP? ? OR PLASMA(2N)(DISPLAY???? OR PANEL????? OR MATRI???? OR SCREEN? ?) OR TFT? ? OR THIN()FILM()TRANSISTOR OR FET? ? OR FIELD()EFFECT()TRANSISTOR? ?
S2	40108455	S INSPECT????? OR DETERMIN??????? OR MEASUR????????? OR TEST?????? OR ESTIMAT????? OR ANALY?????????? OR MONITOR??????? OR CHECK????? OR ASSESS????????? OR EXAM??????????
S3	275756	S (SIGNAL???? OR INFORMATION OR DATA OR PHAS??????? OR INFO)(3N)(WIRE? ? OR WIRING OR FLEX???? OR LINE? ? OR TRAC??????)
S4	45936	S ESD? ? OR GESD? ? OR DESD? ? OR ELECTROSTATIC?????(3N)(DISCHARG????? OR PROTECT????? OR DAMAG?????? OR DEFECT????? OR DISTURB?????? OR FLAW? ?) OR ELECTROSTATIC????(3N)(DEVICE? ? OR APPARATUS OR APPT? ? OR MEANS)
S5	211158	S (CONDUCT???????? OR SHORT????)(3N)(BAR? ? OR ROD? ? OR ELECTROD???? OR ANOD???? OR CATHOD????? OR PROB??????? OR PLATE? ? OR LINE? ? OR TRAC?????) OR GSL? ? OR DSL? ? OR GATE()SHORT????()LINE? ?
S6	215167	S (CURRENT OR VOLT?????)(3N)(PATH????? OR COURS????? OR LINE? ? OR DIRECT????? OR TRACK?????? OR TRAIL???? OR ROUT?????)
S7	8363786	S DEFECT?????? OR IMPERFECT??????? OR STRESS?????? OR BREAK?????? OR FLAW??? OR CRACK???? OR DETERIORAT??? OR DEGRAD??????? OR DECAY?????? OR DECLIN???? OR DEGENERAT????
S8	237197	S (INDIVIDUAL?????? OR SINGL????? OR RESPECTIVE???????? OR SINGULAR????? OR SPECIF?????? OR PARTICULAR????? OR SEPAR???????)(3N)(SHORT???? OR SHORT()CIRCUIT?????? OR END? ? OR POINT? ? OR OPEN()CIRCUIT?????)
S9	0	S S1 AND S2 AND S3 AND S4 AND S5 AND S6 AND S7 AND S8
S10	0	S S1 AND S2 AND S3 AND S4 AND S5 AND S6 AND S7
S11	293	S S1 AND S2 AND S7 AND S4
S12	2	S S11 AND S5
S13	1	RD (unique items)
S14	1	S S11 AND S8
S15	3	S S11 AND S3
S16	3	RD (unique items)
S17	5	S S11 AND S6
S18	5	RD (unique items)

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S19	3	S S18 AND PY<=2003
S20	0	S S1 AND S4 AND S5 AND S8
S21	12	S S1 AND S4 AND S5
S22	11	RD (unique items)
S23	11	S S22 AND PY<=2003
S24	0	S S1 AND S3 AND S4 AND S5
S25	0	S S1 AND S3 AND S5 AND S8
S26	19	S S1 AND S3 AND S5 AND S7
S27	9	RD (unique items)
S28	8	S S27 AND PY<=2003
S29	1	S S14 NOT S13
S30	3	S S16 NOT (S13 OR S14)
S31	3	S S19 NOT (S13 OR S14 OR S16)
S32	10	S S23 NOT (S13 OR S14 OR S16 OR S19)
S33	8	S S28 NOT (S13 OR S14 OR S16 OR S19 OR S23)

30/9/1 (Item 1 from file: 6) **Links**
Fulltext available through: Check for PDF Download Availability and Purchase
NTIS
1340957 **NTIS Accession Number:** NTN87-1157

Transient Protection of Electronic Circuits: Report reviews protection from different forms of electromagnetic pulses

(NTIS Tech Note)
Department of the Air Force, Washington, DC.
Corporate Source Codes: 000260000

Dec 87 1p
Language: English
Journal Announcement: GRAI8804
FOR ADDITIONAL INFORMATION: Detailed information about the technology described may be obtained by ordering the NTIS report order number: AD-A178945/2/NAC, price code: A10.
NTIS Prices: Not available NTIS
Country of Publication: United States

This citation summarizes a one-page announcement of technology available for utilization. Because many modern semiconductor devices (small signal transistors, integrated circuits) can be damaged by potential differences that exceed about 20 to 40 V, the survivability of modern electronics is limited. Modern electronic technology has tended to produce smaller and faster semiconductor devices, particularly high-speed digital logic, microprocessors, metal-oxide-semiconductor (MOS) memories for computers, and GaAs **field effect transistors (FETs)** for microwave use. This progress has led to an increased vulnerability of modern circuits to damage by transient overvoltages, because of the inability of small components to conduct large currents. Electromagnetic pulses from nuclear weapons, lightning, and **electrostatic discharge** are three **examples** of such electrical overstress. Such overstress can cause failure, permanent **degradation**, or temporary malfunction (upset) of electronic devices and systems. This problem and general solutions have been reviewed in a technical report. Nonlinear components and circuits for protection for electrical overstress are discussed in detail, emphasizing spark gaps, metal oxide varistors, and avalanche diodes. However, other components, such as semiconductor diodes, thyristors, resistors, inductors, and optoisolators are also discussed. Applications of these nonlinear components are discussed in the context of **signal lines**, AC power **lines**, and DC power supplies. A final chapter discusses specific upset protection circuits.

Descriptors: *Circuit protection; *Electromagnetic pulses
Identifiers: *Transient radiation effects; NTISNTND
Section Headings: 49B (Electrotechnology--Circuits)

32/9/8 (Item 2 from file: 95) **Links**
TEME-Technology & Management

01082618 E97031037048
Interconnects for device ESD protection

(Kurzschlussverbindung zum Schutz von Bauelementen vor elektrostatischer Entladung)
Jarrett, T; Unger, B
Guidant St. Paul, USA; CRO-BAR Monmouth Beach, USA
Electrical Overstress/Electrostatic Discharge Symp. Proc. 1996, Orlando, USA, Sep 10-12, 1996 , **1996**
Document type: Conference paper **Language:** English
Record type: Abstract
ISBN: 1-878303-69-4

Abstract:
A **conductive** spring loaded **shorting bar** on the leads of a TO-220 MOSFET was found to protect it from **ESD** failures. The MOSFET is used in a medically implantable device where quality and reliability is essential. Pre-production samples revealed significant **ESD** failures, thought to be associated with a mechanical shearing operation. Analysis suggests CDM failures, since testing revealed a low CDM threshold. A custom designed removable shorting interconnect raised all **ESD** thresholds by at least an order of magnitude. No failures have occured in thousands of devices used since the interconnect was incorporated.

Descriptors: CARDIAC PACEMAKERS; ELECTROSTATIC CHARGING; METAL OXIDE SEMICONDUCTOR **FET**; SHORT CIRCUIT; ELECTRIC CONTACTS; **ELECTROSTATIC DISCHARGE**; PRODUCT QUALITY
Identifiers: Herzschrittmacher; elektrostatischer MOSFET-Entladungsschutz

33/9/2 (Item 2 from file: 2) **Links**
INSPEC

06658128 **INSPEC Abstract Number:** B9709-2240-014
Title: Adhesive and conductive adhesive flip chip bonding
Author Zenner, R.L.D.; Connell, G.; Gerber, J.A.
Author Affiliation: 3M Co., St. Paul, MN, USA
Conference Title: Proceedings. 3rd International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces (Cat. No.97TH8263) p. 117-19
Publisher: IEEE , New York, NY, USA
Publication Date: 1997 **Country of Publication:** USA viii+183 pp.
ISBN: 0 7803 3818 9 **Material Identity Number:** XX97-00693
Conference Title: Proceedings 3rd International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces
Conference Sponsor: Int. Microelectron. & Packaging Soc. (IMAPS); IEEE Components, Packaging, & Manuf. Technol. Soc.; Georgia Inst. Technol., Pakcaging Res. Center (PRC)
Conference Date: 9-12 March 1997 **Conference Location:** Braselton, GA, USA

Language: English **Document Type:** Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: Over the past decade the use of adhesives for electronic interconnect has been driven by the explosive growth of **flat panel liquid crystal displays (LCD)**. Developed and used primarily by Japanese manufacturers of consumer products, particle-loaded adhesive films fulfilled a need in **LCDs** that could not be met by solder reflow: low temperature, high line density (to 50 mu m pitch) electrical interconnect to indium tin oxide (ITO) traces on glass. Adhesives may also be used for flip-chip assembly. The advantages of flip-chip attach technology are the same for solder or adhesive technology: footprint reduction, low interconnect resistance, **short signal line** length, and elimination of single-chip packaging costs. Lower parasitics decrease rise times and decrease power requirements. To prevent differential thermal expansion induced solder fatigue, flip-chip attachment using solder reflow requires the use of an underfill adhesive applied in a separate time-consuming process. Adhesive films described in this paper inherently provide an underfill, serve as environmental protection for the chip face, as well as make a solderless electrical connection. Performance results for fine pitch chips have shown stable interconnect resistance below 10 m Omega for bumped chip applications and approximately 100 m Omega with unbumped chip test vehicles. The adhesive flip-chip bonding process and environmental **stress** results will be presented in this paper. (2 Refs)
Subfile: B
Descriptors: adhesion; fine-pitch technology; flip-chip devices
Identifiers: adhesive; flip chip bonding; conductive adhesive; **flat panel liquid crystal display**; particle-loaded adhesive; fine pitch technology; underfill adhesive film; electric interconnect resistance ; environmental **stress**; 50 micron; 10 mohm; 100 mohm
Class Codes: B2240 (Microassembly techniques)
Numerical Indexing: size 5.0E-05 m; resistance 1.0E-02 ohm; resistance 1.0E-01 ohm

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6/15/2006 2:49:01 PM

[File 344] Chinese Patents Abs Jan 1985-2006/Jan
[File 347] JAPIO Nov 1976-2005/Sep(Updated 060103)
[File 350] Derwent WPIX 1963-2006/UD,UM &UP=200607
[File 371] French Patents 1961-2002/BOPI 200209

Set	Items	Description
S1	1235628	S LCD? ? OR LIQUID()CRYSTAL()(DISPLAY????? OR PANEL????? OR MATRI????? OR SCREEN? ?) OR (FLAT OR PASSIVE OR ACTIVE)(2N)(DISPLAY???? OR PANEL???? OR MATRI???? OR SCREEN? ?) OR LIQUID(2N)CRYSTAL OR LCM OR DISPLAY(2N)(MEANS OR DEVICE? ? OR APPARATUS OR APPT? ?) OR FED? ? OR FIELD()(EMIS????? OR EMIT?????)()(DISPLAY????? OR PANEL????? OR MATRI??????? OR SCREEN? ?) OR PDP? ? OR PLASMA(2N)(DISPLAY???? OR PANEL????? OR MATRI???? OR SCREEN? ?) OR TFT? ? OR THIN()FILM()TRANSISTOR OR FET? ? OR FIELD()EFFECT()TRANSISTOR? ?
S2	4244110	S INSPECT????? OR DETERMIN??????? OR MEASUR????????? OR TEST?????? OR ESTIMAT????? OR ANALY?????????? OR MONITOR??????? OR CHECK????? OR ASSESS????????? OR EXAM??????????
S3	286788	S (SIGNAL???? OR INFORMATION OR DATA OR PHAS??????? OR INFO)(3N)(WIRE? ? OR WIRING OR FLEX???? OR LINE? ? OR TRAC??????)
S4	29893	S ESD? ? OR GESD? ? OR DESD? ? OR ELECTROSTATIC?????(3N)(DISCHARG????? OR PROTECT????? OR DAMAG?????? OR DEFECT????? OR DISTURB?????? OR FLAW? ?) OR ELECTROSTATIC????(3N)(DEVICE? ? OR APPARATUS OR APPT? ? OR MEANS)
S5	168471	S (CONDUCT???????? OR SHORT????)(3N)(BAR? ? OR ROD? ? OR ELECTROD???? OR ANOD???? OR CATHOD????? OR PROB??????? OR PLATE? ? OR LINE? ? OR TRAC?????) OR GSL? ? OR DSL? ? OR GATE()SHORT????()LINE? ?
S6	139035	S (CURRENT OR VOLT?????)(3N)(PATH????? OR COURS????? OR LINE? ? OR DIRECT????? OR TRACK?????? OR TRAIL???? OR ROUT?????)
S7	1412819	S DEFECT?????? OR IMPERFECT??????? OR STRESS?????? OR BREAK?????? OR FLAW??? OR CRACK???? OR DETERIORAT??? OR DEGRAD??????? OR DECAY?????? OR DECLIN???? OR DEGENERAT????
S8	162300	S (INDIVIDUAL?????? OR SINGL????? OR RESPECTIVE???????? OR SINGULAR????? OR SPECIF?????? OR PARTICULAR????? OR SEPAR???????)(3N)(SHORT???? OR SHORT()CIRCUIT?????? OR END? ? OR POINT? ? OR OPEN()CIRCUIT?????)
S9	88892	S IC=(G01R-031/00 OR G02F-001/13)
S10	9045	S MC=(S01-G04C OR S01-G09 OR S02-J04A3A OR U11-F01D3 OR U14-K01A8)
S11	0	S S1 AND S2 AND S3 AND S4 AND S5 AND S6 AND S7
S12	8	S S1 AND S2 AND S7 AND S4 AND S5
S13	5	S S12 AND PY<=2003
S14	1	S S1 AND S2 AND S3 AND S4 AND S8
S15	23	S S1 AND S4 AND S5 AND S7
S16	18	S S15 AND PY<=2003
S17	2	S S1 AND S2 AND S3 AND S4 AND S6
S18	1	S S16 AND S9
S19	0	S S16 AND S10
S20	0	S S1 AND S2 AND S3 AND S4 AND S5 AND S6
S21	19925	S S1 AND S2 AND S7
S22	1875	S S21 AND S9
S23	359	S S22 AND S10
S24	75	S S21 AND S4
S25	7	S S24 AND S9
S26	1	S S24 AND S10
S27	4	S S3 AND S4 AND S5 AND S8
S28	4	S S27 AND PY<=2003
S29	5	S S25 AND PY<=2003
S30	2	S S17 NOT S14
S31	1	S S18 NOT (S14 OR S17)
S32	1	S S26 NOT (S14 OR S17 OR S18)
S33	3	S S28 NOT (S14 OR S17 OR S18 OR S26)
S34	4	S S29 NOT (S14 OR S17 OR S18 OR S26 OR S28)
S35	4	S S13 NOT (S14 OR S17 OR S18 OR S26 OR S28 OR S29)
S36	13	S S16 NOT (S13 OR S14 OR S17 OR S18 OR S26 OR S28 OR S29)

14/9/1 (Item 1 from file: 347) **Links**
JAPIO

04994649 **Image available**
THIN FILM TRANSISTOR ARRAY AND ITS INSPECTION METHOD

Pub. No.: 07-287249 [JP 7287249 A]
Published: October 31, 1995 (19951031)
Inventor: NISHIKI TAMAHIKO
OGURA SHIGEKI
YOSHIZAWA YOSHIYO
Applicant: OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
Application No.: 06-080081 [JP 9480081]
Filed: April 19, 1994 (19940419)
International Class: [6] G02F-001/136; G02F-001/1343; H01L-021/66; H01L-029/786
JAPIO Class: 29.2 (PRECISION INSTRUMENTS -- Optical Equipment); 42.2 (ELECTRONICS -- Solid State Components); 46.2 (INSTRUMENTATION -- **Testing**)
JAPIO Keyword: R011 (LIQUID CRYSTALS); R096 (ELECTRONIC MATERIALS -- Glass Conductors)

ABSTRACT
PURPOSE: To provide the **TFT** array with a short-circuiting wire and its **inspection** method which enables the **inspection** of a short circuit between layers by simple conduction **inspection** after the **TFT** array is completed.

CONSTITUTION: The **thin film transistor** array, which is provided with thin film transistors at respective intersection parts of plural address **lines** and plural **data lines** arranged crossing each other and has a display area having an auxiliary capacity line connected to the thin film transistors and also has a 1st short- circuiting wire arranged outside the display area through an **electrostatic protection** element, is equipped with a short-circuiting **wire** 31 for the **data lines** 12 which is arranged outside the 1st short-circuiting wire 30, a short-circuiting wire 31 for the address lines 11 which is arranged outside the 1st short-circuiting wire 30, and a short-circuiting wire 31 for the auxiliary capacity line 13 connected by the same metallic layer as the short-circuiting wire 31 for the address lines 11; and a discharging stylus is provided as the **electrostatic protecting means** 40 at the **separation** part between the **short- circuiting wire** 32 for the **data lines** 12, and the short-circuiting wire 31 for the address lines 11 and short-circuiting wire 31 for the auxiliary capacity line 13.

31/9/1 (Item 1 from file: 347) **Links**
JAPIO

05985142 **Image available**
MANUFACTURE OF LIQUID CRYSTAL DISPLAY DEVICE

Pub. No.: 10-268242 [JP 10268242 A]
Published: October 09, 1998 (**19981009**)
Inventor: YAMANAKA HIDEO
Applicant: SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
Application No.: 09-074744 [JP 9774744]
Filed: March 27, 1997 (19970327)
International Class: [6] **G02F-001/13**
JAPIO Class: 29.2 (PRECISION INSTRUMENTS -- Optical Equipment)
JAPIO Keyword: R011 (LIQUID CRYSTALS)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a manufacturing method of a **liquid crystal display device** preventing an **electrostatic damage**, preventing metallic dust caused by a probe test as it is from sticking on a **liquid crystal** drive substrate and thus, preventing **deterioration** in yield and quality caused by the sticking of the metallic dust.

SOLUTION: A **liquid crystal** drive substrate 1 forming a **conductive short line short**-circuiting all **electrode** pads in at least a scribed area is provided, and an oriented film 3 is formed on its inner surface, and succeedingly, rubbing processing of the oriented film 3 is performed. Then, the **liquid crystal** drive substrate 1 is mounted on a dicing sheet 4, and taper shaving processing of a V groove 6 in the scribe area of the **liquid crystal** drive substrate 1 in its state is performed, and the **short line** in the scribe area is removed, and the **short** circuit between the **electrode** pads is released. Then, the **liquid crystal** drive substrate 1 in the state as it is mounted on the dicing sheet 4 is probe tested. Thereafter, taper shaving process parts are full-cut diced.

33/9/2 (Item 1 from file: 350) **Links**
Derwent WPIX

015238768 **Image available**
WPI Acc No: 2003-299694/**200329**
XRPX Acc No: N03-238455

Electrostatic discharge protection circuit for thin film transistor liquid crystal display, uses ESD protection units to connect gate shorting line to data shorting line and to connect data shorting line to common electrode

Patent Assignee: LG PHILIPS LCD CO LTD (GLDS); KIM Y (KIMY-I); LEE H (LEEH-I)
Inventor: KIM Y; LEE H; KIM Y G; LEE H G
Number of Countries: 006 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030020845	A1	20030130	US 2002180979	A	20020627	200329	B
DE 10228517	A1	20030306	DE 10228517	A	20020626	200329	
JP 2003107528	A	20030409	JP 2002190048	A	20020628	200333	
KR 2003005797	A	20030123	KR 200141251	A	20010710	200334	
CN 1396656	A	20030212	CN 2002140347	A	20020628	200335	
KR 386849	B	20030609	KR 200141251	A	20010710	200367	
TW 575766	A	20040211	TW 2002113993	A	20020626	200454	
US 6791632	B2	20040914	US 2002180979	A	20020627	200460	

Abstract (Basic): US 20030020845 A1

NOVELTY - An **electrostatic discharge (ESD) protection** unit that connects **gate shorting line** to **data shorting line** and another **ESD** protection unit that directly connects the **data shorting line** to a common electrode (ITO), are provided along with **ESD** protection units for connecting respective gate **lines** to **gate shorting line** and **data lines** to **data shorting line**, **respectively.**

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for method of protecting liquid crystal display **device** from **electrostatic discharge**.

USE - For **electrostatic discharge (ESD) protection** of thin film transistors liquid crystal display (TFT-LCD).

ADVANTAGE - Distributes more stable and efficient dispersion of static electric charges into and from the **data lines**.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic circuit diagram of the **electrostatic discharge protection** circuit.

pp; 10 DwgNo 4/6

34/9/4 (Item 1 from file: 350) **Links**
Derwent WPIX

013148035 **Image available**
WPI Acc No: 2000-319907/**200028**
Related WPI Acc No: 2004-798418
XRPX Acc No: N00-240117

Semiconductor device for liquid crystal panel with thin film transistors and photoelectric conversion apparatus has common electrode bias line, several gate lines and several transfer lines electrically connected

Patent Assignee: CANON KK (CANO); KAIFU N (KAIF-I); MOCHIZUKI C (MOCH-I); WATANABE M (WATA-I)
Inventor: KAIBU K; MOCHITSUKI T; WATANABE S; KAIFU N; MOCHIZUKI C; WATANABE M
Number of Countries: 028 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 993038	A1	20000412	EP 99306846	A	19990827	200028 B
JP 2000148044	A	20000526	JP 99235770	A	19990823	200033
CN 1254187	A	20000524	CN 99118343	A	19990831	200043
US 20030111664	A1	20030619	US 99384424	A	19990827	200341
			US 2002305981	A	20021129	
US 6586769	B1	20030701	US 99384424	A	19990827	200345
US 20050051779	A1	20050310	US 99384424	A	19990827	200519
			US 2002305981	A	20021129	
			US 2004969875	A	20041022	
US 6909116	B2	20050621	US 99384424	A	19990827	200543
			US 2002305981	A	20021129	
CN 1144292	C	20040331	CN 99118343	A	19990831	200610
US 20060087577	A1	20060427	US 99384424	A	19990827	200629
			US 2002305981	A	20021129	
			US 2004969875	A	20041022	
			US 2005297414	A	20051209	

Priority Applications (No Type Date): JP 99235770 A 19990823; JP 98246151 A 19980831
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 993038	A1	E	21	H01L-021/84	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2000148044	A		12	G09F-009/30	
CN 1254187	A			H01L-027/10	
US 20030111664	A1			G02F-001/1343	Div ex application US 99384424
US 6586769	B1			H01L-029/04	
US 20050051779	A1			H01L-029/04	Div ex application US 99384424 Div ex application US 2002305981 Div ex patent US 6586769

US 6909116	B2	H01L-029/04	Div ex application US 99384424 Div ex patent US 6586769
CN 1144292	C	H01L-027/10	
US 20060087577	A1	G02F-001/13	Div ex application US 99384424 Div ex application US 2002305981 Div ex application US 2004969875 Div ex patent US 6586769 Div ex patent US 6909116

Abstract (Basic): EP 993038 A1

NOVELTY - A gate of each of the number of thin film transistors is connected to a corresponding one of a number of gate lines. The other of the source and the drain of each of the number of thin film transistors are connected to a corresponding transfer line and common electrode bias line. The gate lines and the transfer lines are electrically connected.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) a substrate carrying a matrix array of rows and columns of switching elements such as thin film transistors;

(b) an array for **liquid crystal display** or image sensing apparatus.

USE - For a **liquid crystal panel** with **TFTs** and a photoelectric conversion apparatus.

ADVANTAGE - Can effectively prevent **electrostatic defects** (**ESD**) during manufacture processes and improve a manufacture yield. Can maintain the effects of preventing **ESD** until the panel is finally mounted on an apparatus, by electrically connecting wiring lines by resistors. A number of thin film transistors and associated wiring lines are formed on a substrate, in which the wiring lines are disposed vertically and horizontally crossing each other, the wiring lines are electrically insulated at each cross point

DESCRIPTION OF DRAWING(S) - The drawing is a simplified **example** of a semiconductor device of this invention.

pp; 21 DwgNo 1/11

Title Terms: SEMICONDUCTOR; DEVICE; LIQUID; CRYSTAL; PANEL; THIN; FILM; TRANSISTOR; PHOTOELECTRIC; CONVERT; APPARATUS; COMMON; ELECTRODE; BIAS; LINE; GATE; LINE; TRANSFER; LINE; ELECTRIC; CONNECT

Derwent Class: P81; U13; U14

International Patent Class (Main): **G02F-001/13**; G02F-001/1343; G02F-001/136; G09F-009/30; H01L-021/84; H01L-027/10; H01L-029/04

International Patent Class (Additional): G02F-001/133; G02F-001/1365; H01L-021/822; H01L-021/86; H01L-023/48; H01L-027/02; H01L-027/04; H01L-029/786; H01L-031/20

File Segment: EPI; EngPI

Manual Codes (EPI/S-X): U13-E01; U14-H01A; U14-K01A1B; U14-K01A2B

35/9/1 (Item 1 from file: 347) **Links**
JAPIO

06061333 **Image available**

ACTIVE MATRIX LIQUID CRYSTAL DISPLAY DEVICE

Pub. No.: 11-002839 [JP 11002839 A]
Published: January 06, 1999 (**19990106**)
Inventor: HIROSHIMA MINORU
ISODA TAKASHI
Applicant: HITACHI LTD
HITACHI DEVICE ENG CO LTD
Application No.: 09-152342 [JP 97152342]
Filed: June 10, 1997 (19970610)
International Class: G02F-001/136; G02F-001/1345; G09F-009/30; H01L-029/786

ABSTRACT

PROBLEM TO BE SOLVED: To provide the **active matrix liquid crystal display device** which can actualize short-circuit **inspection** between signal **lines** through a **short bar** and is equipped with **electrostatic protecting** circuit constitution capable of preventing problems of dielectric **breakdown** caused at an intersection part between the common line and a signal line of an **electrostatic protecting** circuit.

SOLUTION: **Short bars** SHde and SHdo of **electrostatic protecting** circuits of electrically independent even-numbered signal lines (group) D2j and odd- numbered signal lines (group) D2j-1 are coupled by a coupling element part CONEL consisting of a nonlinear element or high-resistance element and thus placed in an electrically connected state from a floating state. Consequently, both the even-numbered and odd-numbered **electrostatic protecting** circuit systems are held at the same potential and the intersection parts between the signal lines and common line are held at the same potential to prevent dielectric **breakdown**.

35/9/3 (Item 1 from file: 350) **Links**
Derwent WPIX

010048648 **Image available**
WPI Acc No: 1994-316359/**199439**
XRPX Acc No: N94-248480

Electrostatic discharge protection method for processing active matrix liquid crystal display - using shorting conductor or bar, at external lead contact areas, to short out or to connect to one another, all row and column contacts on display

Patent Assignee: HONEYWELL INC (HONE)
Inventor: DODD S R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5353142	A	19941004	US 9355047	A	19930429	199439	B

Priority Applications (No Type Date): US 9355047 A 19930429
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5353142	A		5	G02F-001/1343	

Abstract (Basic): US 5353142 A

The method includes the step of cutting at least one slot on a second surface into a first plane, the slot being approximately perpendicular to the second surface. The slot has a depth that goes through a portion of the first plane and the slot is about from two to four mils from the first surface of the first plane. The slot has a location proximate to the lead contacts in an area between a shorting conductor and a central area of the first plane. The first plane has a peripheral area extending from the slot to the perimeter of the first plane.

The peripheral area is removed from the first plane, after any desired external connection or attachment to the lead contacts at points between the slot and the central area, any fabrication of the display and any installation of any polarizer, by **breaking** off the peripheral area at the location of the slot, thus, removing the shorting conductor from the display.

ADVANTAGE - Allows **shorting bar** to remain in contact with display's external leads through all of processing steps until display **testing** is ready to commence.

Dwg.1a/1

Title Terms: ELECTROSTATIC; DISCHARGE; PROTECT; METHOD; PROCESS; ACTIVE; MATRIX; LIQUID; CRYSTAL; DISPLAY; SHORT; CONDUCTOR; BAR; EXTERNAL; LEAD; CONTACT; AREA; SHORT; CONNECT; ONE; ROW; COLUMN; CONTACT; DISPLAY
Derwent Class: P81; U14
International Patent Class (Main): G02F-001/1343

35/9/4 (Item 2 from file: 350) Links

009823293 **Image available**
WPI Acc No: 1994-103149/**199413**
XRPX Acc No: N94-080533

Electronic device e.g. LCD mfg. method on insulating substrate with thin film circuit elements and connections - using anti-electrostatic discharge shorting links between connection tracks during mfr., which are later broken by pulse of electric current between linked tracks

Patent Assignee: PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS UK LTD (PHIG)
Inventor: YOUNG N D
Number of Countries: 006 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 589519	A2	19940330	EP 93202677	A	19930916	199413 B
JP 6224147	A	19940812	JP 93234959	A	19930921	199437

Priority Applications (No Type Date): GB 9220220 A 19920924
Cited Patents: No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 589519	A2	E	8	G02F-001/136	
Designated States (Regional): DE FR GB IT NL					
JP 6224147	A		6	H01L-021/265	

Abstract (Basic): EP 589519 A

The electronic device mfg. method involves connecting the a group of the device thin film connection tracks to a removable **ESD** path to protect the tracks from **damage** due to **electrostatic discharge**. The removable **ESD** path is conductive thin film links (6) between the separate thin film tracks (4) of the group.

The tracks (4) and their links may be of, for **example**, aluminium or a metal silicide. The **ESD** path is removed by applying an electrical pulse (8) between the linked tracks (4) to pass a sufficiently large current as to evaporate and **break** the thin film links (6) by Joule heating.

USE/ADVANTAGE - E.g. image sensor or data store with switching matrix. Provides **ESD** protection during mfr. e.g. during ion implantation; avoids damage caused by alternative cutting methods e.g. scribing or laser.

Dwg.2/5

Title Terms: ELECTRONIC; DEVICE; **LCD**; MANUFACTURE; METHOD; INSULATE; SUBSTRATE; THIN; FILM; CIRCUIT; ELEMENT; CONNECT; ANTI; ELECTROSTATIC; DISCHARGE; SHORT; LINK; CONNECT; TRACK; MANUFACTURE; LATE; **BREAK**;

36/9/2 (Item 2 from file: 347) **Links**
JAPIO

06296049 **Image available**

LIQUID CRYSTAL DISPLAY DEVICE, ITS PRODUCTION AND DETECTING METHOD OF DEFECT

Pub. No.: 11-237641 [JP 11237641 A]
Published: August 31, 1999 (**19990831**)
Inventor: KIM DONG-GYO
LEE SANG-KYUNG
BUN BINKYO
Applicant: SAMSUNG ELECTRONICS CO LTD
Application No.: 10-346844 [JP 98346844]
Filed: December 07, 1998 (19981207)
Priority: 9766154 [KR 66154], KR (Korea) Republic of, December 05, 1997 (19971205)
9849389 [KR 49389], KR (Korea) Republic of, November 18, 1998 (19981118)
International Class: G02F-001/1343; G02F-001/136

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **thin film transistor** substrate having **short bars** which make detection of short circuit fault easy and which are not **damaged** by **electrostatic** charges by arranging plural first wirings parallel to one another, plural second wirings formed parallel to the first wirings, first and second **short bars** connected to the first and second wirings, and main **short bars** formed outside the first and second **short bars**.

SOLUTION: First and second auxiliary **short bars** 410, 420 are formed between a gate **short bar** 200 and gate pads 110, 120 and parallel to the gate **short bar** 200. Third to fifth subshort bars 210, 220, 230 are formed between a data **short bar** 400 and data pads 510, 520 and parallel to the data **short bar** 400. In this structure. the first and second auxiliary **short bars** 410, 420 are connected to G1, G3, and G2, G4, respectively. The third to fifth auxiliary **short bars** 210, 220, 230 are connected to data lines D1 and D4, D2, D3, respectively.

36/9/3 (Item 3 from file: 347) **Links**
JAPIO

05622253 **Image available**
MANUFACTURING METHOD OF ACTIVE MATRIX DISPLAY DEVICE

Pub. No.: 09-237053 [JP 9237053 A]
Published: September 09, 1997 (**19970909**)
Inventor: SUZUKI KOJI
Applicant: TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
Application No.: 09-055219 [JP 9755219]
Filed: March 10, 1997 (19970310)
International Class: [6] G09F-009/30; G02F-001/136; G09F-009/00
JAPIO Class: 44.9 (COMMUNICATION -- Other); 29.2 (PRECISION INSTRUMENTS -- Optical Equipment)
JAPIO Keyword: R004 (PLASMA); R011 (LIQUID CRYSTALS)

ABSTRACT

PROBLEM TO BE SOLVED: To fully prevent the **device** from **electrostatic breakage** during and after assembling.

SOLUTION: In the manufacturing method of a **display device** which drives **display** cells by an **active matrix** substrate which has plural row lines A, plural column lines crossing these row lines, and switching elements C each at the crossing points between these row lines and column lines, during and after assembling, a **short**-circuit **line** GL is laid in the peripheral section of the **active matrix** substrate. The end section of each of the row lines and the column lines is connected to the **short**-circuit **line** GL through a resistor.

36/9/5 (Item 5 from file: 347) **Links**
JAPIO

04601883 **Image available**
LIQUID CRYSTAL DISPLAY DEVICE AND ITS MANUFACTURE

Pub. No.: 06-273783 [JP 6273783 A]
Published: September 30, 1994 (**19940930**)
Inventor: KANEDA YOSHIHIRO
Applicant: CITIZEN WATCH CO LTD [000196] (A Japanese Company or Corporation), JP (Japan)
Application No.: 05-086952 [JP 9386952]
Filed: March 23, 1993 (19930323)
International Class: [5] G02F-001/1343; G02F-001/133; G02F-001/1345
JAPIO Class: 29.2 (PRECISION INSTRUMENTS -- Optical Equipment)
JAPIO Keyword: R011 (LIQUID CRYSTALS)
Journal: Section: P, Section No. 1849, Vol. 18, No. 688, Pg. 162, December 26, 1994 (19941226)

ABSTRACT

PURPOSE: To prevent an electrode pattern used for display from being **damaged** by **electrostaticity** and also to make it possible to detect a **defective short**-circuit between each **electrode** pattern, as to a method for manufacturing a **liquid crystal display device**.

CONSTITUTION: The electrode pattern 20 used for display is formed on a substrate 10, a common electrode 30 and a connection wire 40 are arranged by use of the same conductive film. The electrostaticity charged on each electrode pattern 20 at the manufacturing process of the **liquid crystal display device** attains the same potential through the common electrode 30, so that the **breakdown** caused by the discharge between the electrode patterns 20 is not generated, and also, the **defective** short-circuit is detected with the resistance value of the connection wire 40.

36/9/12 (Item 5 from file: 350) **Links**
Derwent WPIX

004349236
WPI Acc No: 1985-176114/**198529**
XRPX Acc No: N85-132217
Electrostatic discharge resistive connector system - includes short-circuiting bar to protect FET from charges introduced when device is plugged in by consumer

Patent Assignee: ANONYMOUS (ANON)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
RD 254025	A	19850610				198529	B

Priority Applications (No Type Date): RD 85254025 A 19850520
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
RD 254025	A		1		

Abstract (Basic): RD 254025 A

A **conductive** elastomeric **shorting bar** (12) is provided which short-circuits the terminals of the circuit card until the connector is fully inserted. When it is fully inserted the bar is displaced and no longer provides a short-circuit.

In this way a make-before-**break** system is provided which protects the **FETs** in the equipment.

Title Terms: ELECTROSTATIC; DISCHARGE; RESISTOR; CONNECT; SYSTEM; SHORT; CIRCUIT; BAR; PROTECT; **FET**; CHARGE; INTRODUCING; DEVICE; PLUG; CONSUME
Index Terms/Additional Words: PCB
Derwent Class: U11; V04; X25
International Patent Class (Additional): H05F-000/01; H05K-000/01
File Segment: EPI
Manual Codes (EPI/S-X): U11-D; V04-A09; V04-B01; V04-M05; X25-S